



Dual P-Channel 12-V (D-S) MOSFET

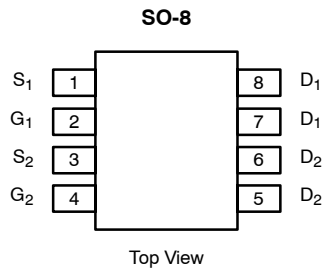
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-12	0.018 @ V _{GS} = -4.5 V	-8.9
	0.022 @ V _{GS} = -2.5 V	-8.1
	0.028 @ V _{GS} = -1.8 V	-3.6

FEATURES

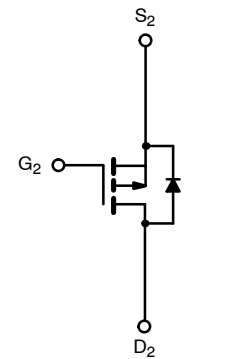
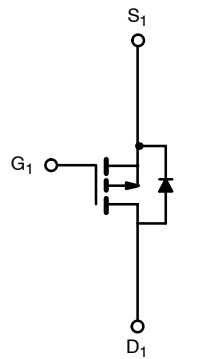
- TrenchFET® Power MOSFET
- Advanced High Cell Density Process

APPLICATIONS

- Load Switching



Ordering Information: Si4931DY—E3
Si4931DY-T1—E3 (with Tape and Reel)



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-12		V	
Gate-Source Voltage	V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	-8.9	-6.7	A
		T _A = 70 °C	-7.1	-5.4	
Pulsed Drain Current	I _{DM}	-30			
continuous Source Current (Diode Conduction) ^a	I _S	-1.7	-0.9		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.0	1.1	W
		T _A = 70 °C	1.3	0.7	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	46	62.5	°C/W
		Steady State	80	110	
Maximum Junction-to-Foot (Drain)	R _{thJF}	24	32		

Notes

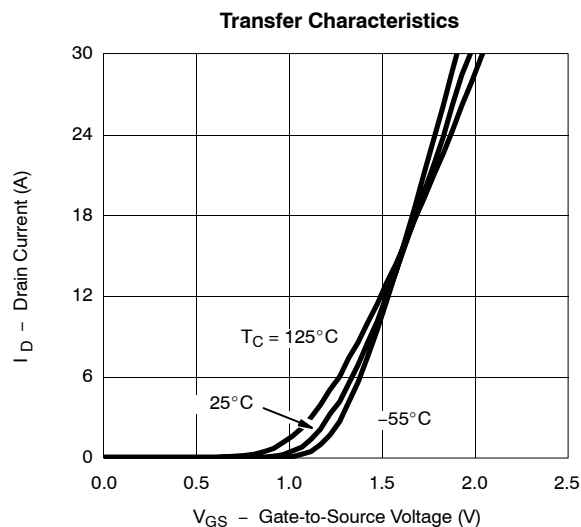
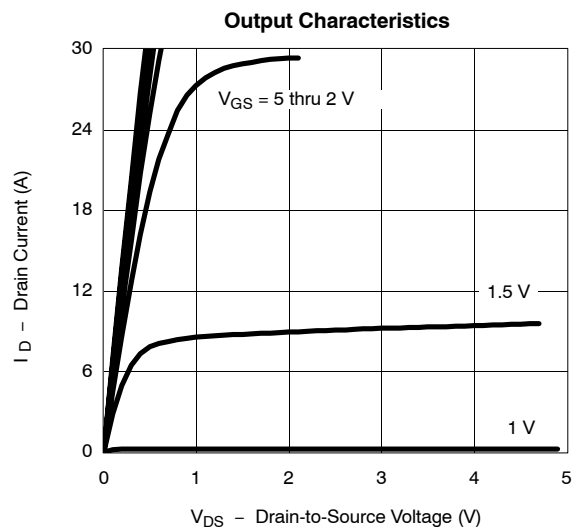
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -350 μA	-0.4		-1.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -12 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -12 V, V _{GS} = 0 V, T _J = 55 °C			-5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -4.5 V	-30			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -4.5 V, I _D = -8.9 A		0.0145	0.018	Ω
		V _{GS} = -2.5 V, I _D = -8.1 A		0.018	0.022	
		V _{GS} = -1.8 V, I _D = -3.6 A		0.023	0.028	
Forward Transconductance ^a	g _{fs}	V _{DS} = -6 V, I _D = -8.9 A		26		S
Diode Forward Voltage ^a	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		-0.7	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -8.9 A		34.5	52	nC
Gate-Source Charge	Q _{gs}			5.1		
Gate-Drain Charge	Q _{gd}			9.6		
Gate Resistance	R _g			9		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -6 V, R _L = 6 Ω I _D ≅ -1 A, V _{GEN} = -4.5 V, R _G = 6 Ω		25	40	ns
Rise Time	t _r			46	70	
Turn-Off Delay Time	t _{d(off)}			230	345	
Fall Time	t _f			155	235	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = -1.7 A, di/dt = 100 A/μs		128	

Notes

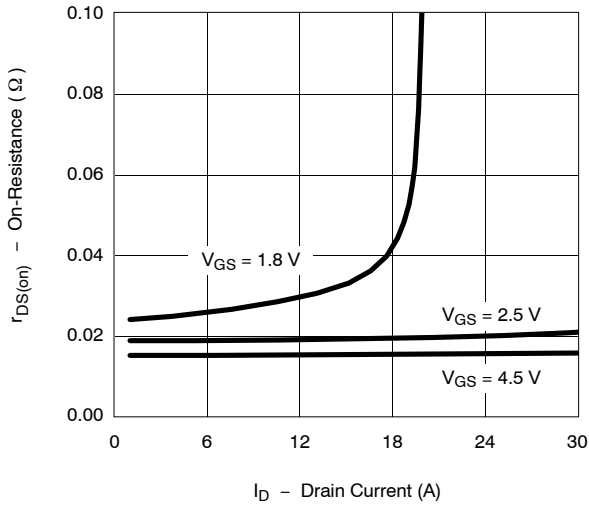
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

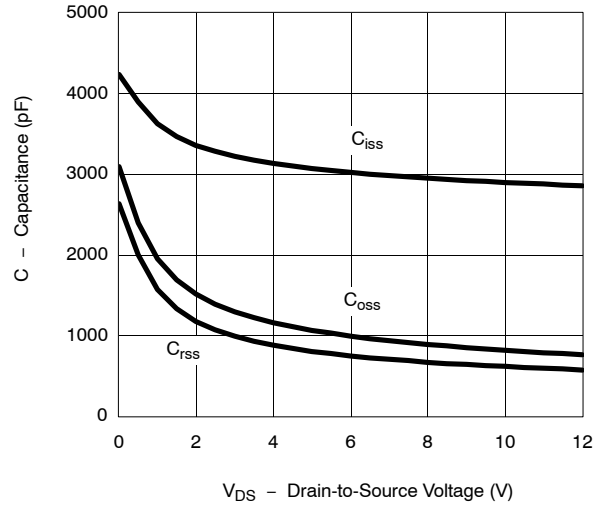


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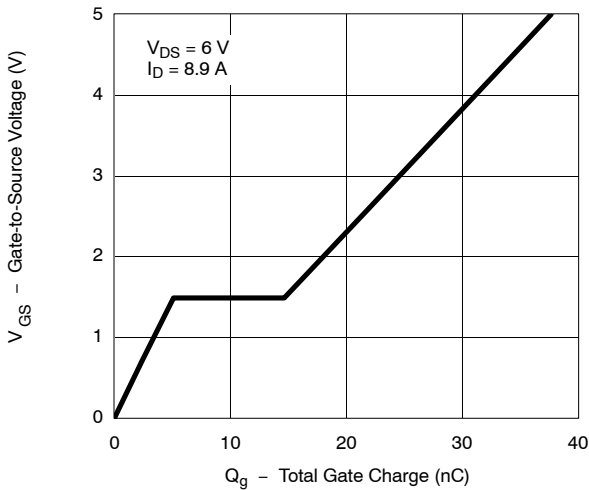
On-Resistance vs. Drain Current



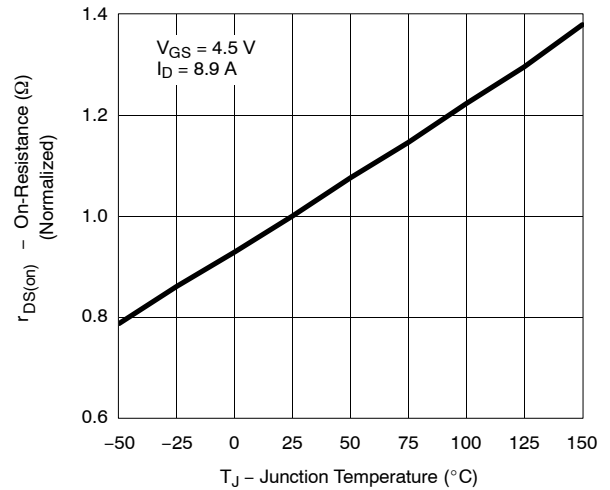
Capacitance



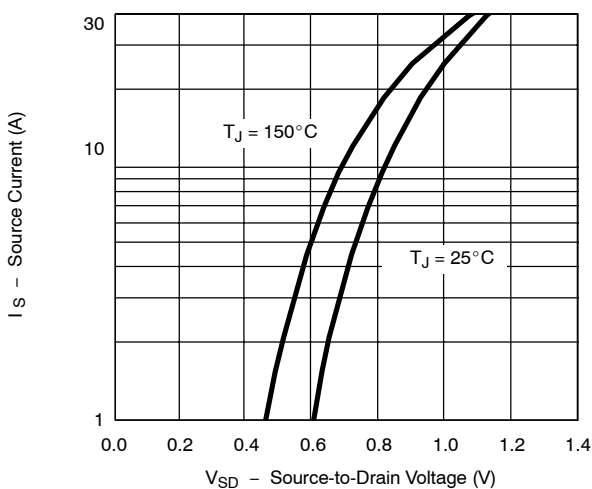
Gate Charge



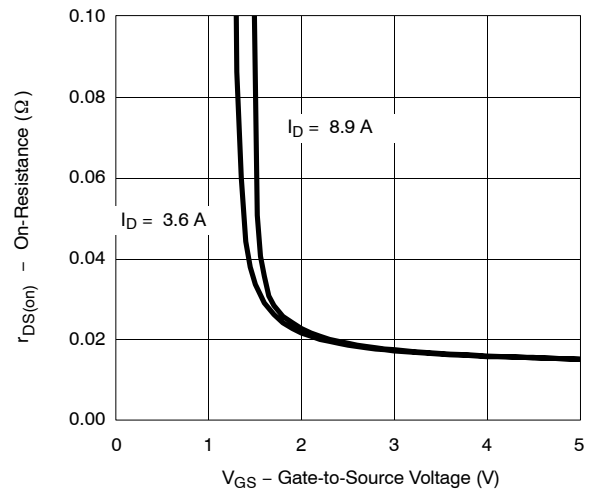
On-Resistance vs. Junction Temperature



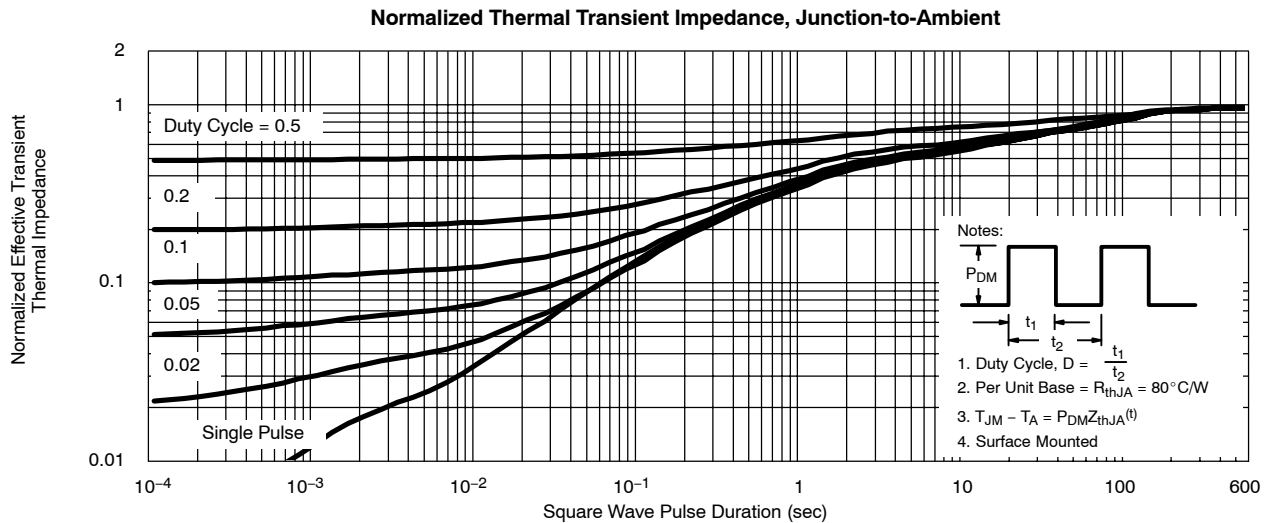
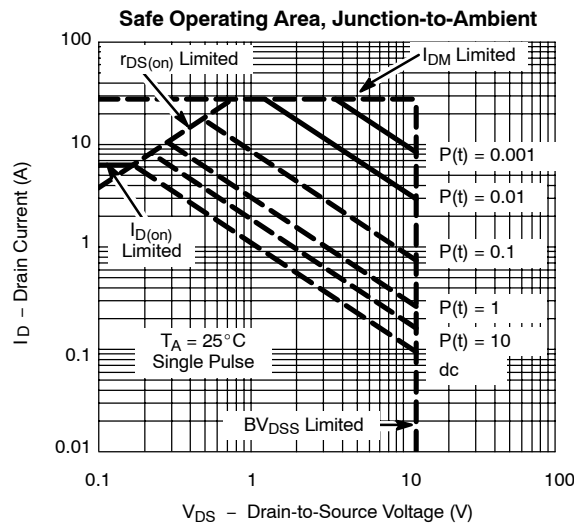
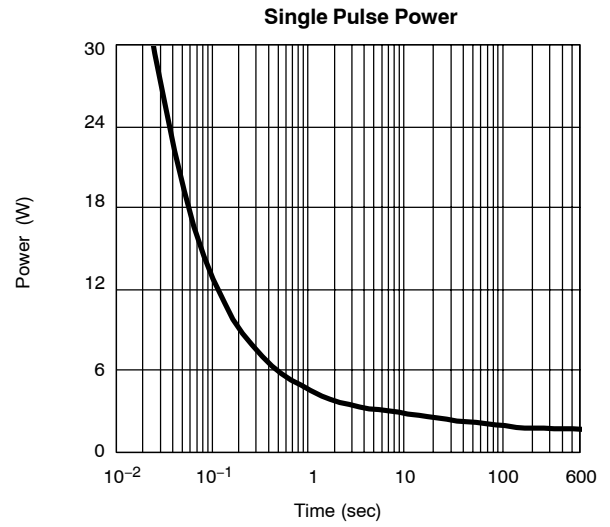
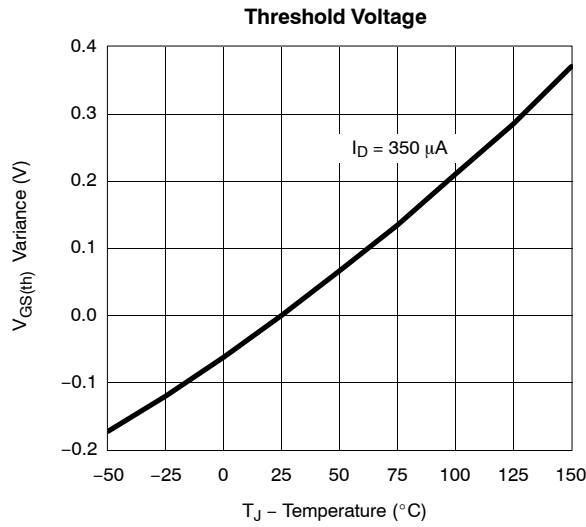
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

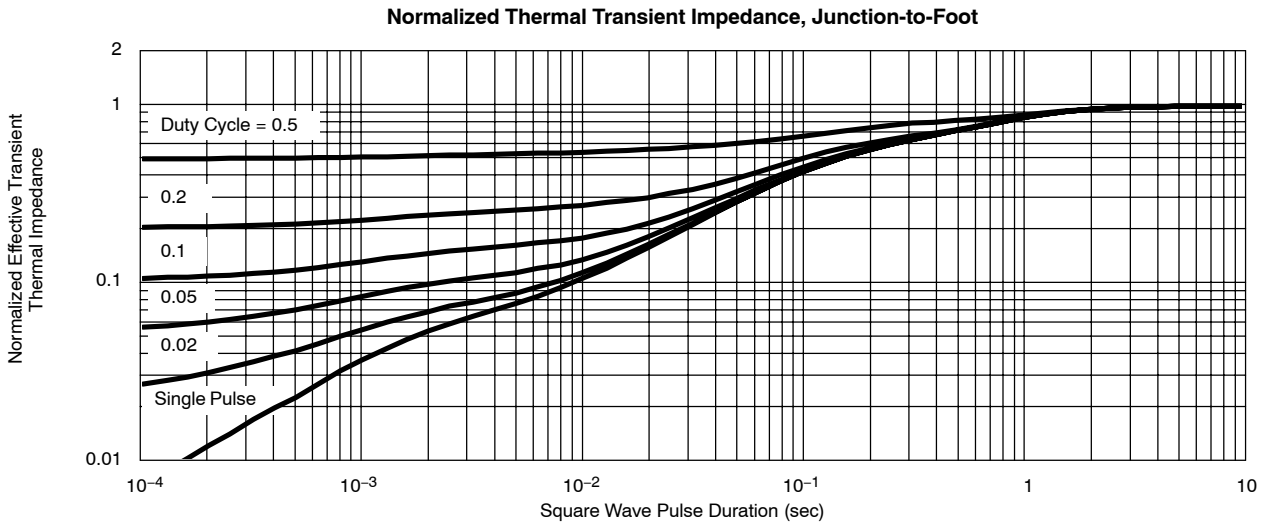


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





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